REMARKS

Claims 1-4 and 7-10 have been amended. Claims 1-10 are pending. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claim 5 stands rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Applicants respectfully traverse the rejection.

Claim 5 depends from claim 1 and amendments to claim 1 should overcome the 35 U.S.C. § 112, second paragraph rejection for lack of antecedent basis.

Claims 1, 6, and 7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Publ. No. 2003/0030444 ("Kogawa et al."). Applicants respectfully traverse the rejection.

Kogawa et al. is directed to a highly sensitive charged particle measuring device capable of measuring low-level alpha rays. Kogawa et al. may have a plurality of semiconductor detectors 1, an adder 31 for adding output signals from the semiconductor detectors, and an analyzer 30e for analyzing the energy range of alpha rays. Kogawa et al. does not disclose, however, "an anticoincidence counter for taking a logical product of a plurality of semiconductor detectors, wherein the anticoincidence counter delays a signal created from the logical product to create a gate signal; a signal corresponding to the gate signal is suppressed from an addition signal obtained by adding outputs from the plurality of semiconductor detectors; and a peak analyzer for analyzing an energy distribution of α-rays based on a signal obtained after suppression of the signal corresponding to the gate signal from the addition signal obtained by adding the outputs from the plurality of semiconductor detectors." Because Kogawa et al. does not disclose, teach or suggest all of the limitations of claim 1, Applicant

respectfully submits that the 35 U.S.C. §102(b) rejection of independent claim 1 and dependent claim 6 should be withdrawn and the claims allowed.

Claim 7 recites an α-ray measuring method comprising, in part, the steps of "taking a logical product of a plurality of said semiconductor detectors using an anticoincidence counter; delaying a signal created from the logical product using said anticoincidence counter to create a gate signal; suppressing a signal corresponding to the gate signal from a signal obtained by adding output signals from said respective semiconductor detectors." Kogawa et al. does not disclose, teach or suggest an anticoincidence counter which takes a logical product of a plurality of semiconductor detectors or delays a signal created from the logical product. Therefore, Applicant respectfully submits that the 35 U.S.C. § 102(b) rejection of claim 7 should be withdrawn and the claim allowed.

Claims 1, 6, and 7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,639,392 ("Kogawa"). Applicants respectfully traverse the rejection.

For the above-mentioned reasons, Applicant respectfully submits that the 35 U.S.C. § 102(e) rejection of claims 1, 6 and 7 be withdrawn and the claims allowed.

Claims 2-4 and 8-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kogawa in view of U.S. Patent No. 3,678,275 ("Schneider"). Applicants respectfully traverse the rejection.

Schneider discloses a signal input to a detector 276 which is suppressed by a signal input to another detector 278. (Schneider, col. 7, lines 20-25). However, Schneider does not disclose the creation of gate signal from a logical product or to add outputs of plurality of semiconductor detectors and use the addition signal as a detection signal. Accordingly, Kogawa and Schneider, even when considered in

combination, fail to teach or suggest all limitations of claims 2-4. For at least this reason, Applicant respectfully requests the withdrawal of rejection of claims 2-4.

Claims 8-10 recite an α-ray measuring method comprising, in part, the steps of "taking a logical product of a plurality of said semiconductor detectors using an anticoincidence counter; delaying a signal created from the logical product using said anticoincidence counter to create a gate signal; suppressing a signal corresponding to the gate signal from a signal obtained by adding output signals."

As mentioned earlier, Kogawa does not disclose, teach or suggest these limitations. Schneider too does not disclose the creation of gate signal from a logical product or to add outputs of plurality of semiconductor detectors. Accordingly, Kogawa and Schneider, even when considered in combination, fail to teach or suggest all limitations of claims 8-10. For at least this reason, Applicant respectfully requests the withdrawal of rejection of claims 8-10.

Moreover, the Office Action contends that although claims 3, 4, 9 and 10 fail "to disclose semiconductor detectors that are positioned on planes one above the other [] such an arrangement would have been obvious to one having ordinary skill in the art . . ." (Office Action, p.5). The burden to prove a *prima facie* case of obviousness is on the Examiner. The examiner must meet the following three criteria for proving a *prima facie* case of obviousness – suggestion or motivation in the references; a reasonable expectation of success; and the reference teach or suggest all claim limitations. MPEP §2143. Here, the Examiner has failed to meet the burden and therefore, for this additional reason, claims 3, 4, 9 and 10 are allowable.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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